02-07-00

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Washington, DC 20231

Attorney Docket: E0545/1516P
PATENT

Sir:

Transmitted herewith for filing is the Patent Application of

Inventors: **Ahmad Ghaemmaghami; Zoran Krivokapic; Brian Swanson**

Claiming Benefit of Prior U.S. Application(s):
Amend the specification by inserting before the first line, the following sentence:
"This application claims the benefit of U.S. Provisional Application No. 60/168,155 filed on November 29, 1999."

For: **METHOD AND SYSTEM FOR PROVIDING HALO IMPLANT TO A SEMICONDUCTOR DEVICE WITH MINIMAL IMPACT TO THE JUNCTION CAPACITANCE**

Enclosed with the Patent Application are:

- X Four (4) sheet(s) of drawings
- X Declaration of Inventors
- X Power of Attorney by Assignee
- X Assignment and Recordation Form
- ___ Information Disclosure Statement (PTO Form 1449).
- X Self Addressed, Stamped Postcard.

The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)	**LARGE ENTITY**	
FOR:	**NO. FILED**	**NO. EXTRA**	RATE	FEE
BASIC FEE				$ 690.00
TOTAL CLAIMS	**14** - 20 =	**0**	x 18 =	$ 0.00
INDEP. CLAIMS	**2** - 3 =	**0**	x 78 =	$ 0.00
__ MULTIPLE DEPENDENT CLAIM PRESENTED				$ 0.00
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X Any additional filing fees required under 37 CFR 1.16.

X Any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

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EXPRESS MAIL CERTIFICATE

I hereby certify that the above paper/fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below and is addressed to the Commissioner of Patents and Trademarks, Washington, DC 20231, on February 3, 2000. Express Mail No. **EL272673280US**. Signature of Person mailing paper/fee:

Joseph A. Sawyer, Jr

UNITED STATES PATENT APPLICATION

FOR

METHOD AND SYSTEM FOR PROVIDING HALO IMPLANT TO A SEMICONDUCTOR DEVICE WITH MINIMAL IMPACT TO THE JUNCTION CAPACITANCE

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METHOD AND SYSTEM FOR PROVIDING HALO IMPLANT TO A SEMICONDUCTOR DEVICE WITH MINIMAL IMPACT TO THE JUNCTION CAPACITANCE

FIELD OF THE INVENTION

The present invention relates to semiconductor devices and more particularly providing a halo implant when manufacturing semiconductor devices.

BACKGROUND OF THE INVENTION

A halo implant is typically utilized to implant dopant on a semiconductor device. In-line lithography or DUV (deep ultra violet) photoresist is typically utilized to mask the halo implant process. Typically, the same mask (lightly doped drain) (LDD) is utilized for the halo implant, since the halo implant takes place after the LDD implant. Due to the chemistry of the photoresist, an implant shadowing problem oftentimes occurs utilizing conventional processes (mask & photoresist set), which adversely affects yield and performance of the devices as manufacturing processes move toward smaller geometries.

The first problem is that the photoresist thickness in the area of implant is of a thickness such that an implant delivered at a 45° angle can result in an asymmetric and leaky transistor. A second problem is the thickness of the photoresist related to the trench oxidation region of the device. Accordingly, if a thick photoresist (0.55μm or greater) is placed over the trench oxidation, due to the soft jelly type nature of the photoresist oftentimes the photoresist will fall and cover areas that are to be implanted. Even if the photoresist stands erect at the smaller process technologies, the halo implant will not reach the targeted areas. In addition, the conventional processes do not typically account for the need for selective doping of the source/drain area.

Accordingly, what is needed is a system and method for overcoming the above-identified problems at smaller process geometrics. The present invention addresses such a need.

SUMMARY OF THE INVENTION

A method and system for providing a halo implant to a semiconductor device is disclosed. The method and system comprises providing a thin photoresist layer to the semiconductor device. The method and system further includes providing the halo implant to the appropriate area of the semiconductor device.

Accordingly, in a system and method in accordance with the present invention, a photo photoresist that is capable of thinner profile, i.e., DUV photoresist is utilized. This will allow one to lower the photoresist thickness to the proposed 1000A (in the field) or lower if the process allows. With this photoresist thickness, taking into account other height variables, the source and drain regions can be opened only as needed.

At a 45° angle, the implant can be delivered to all transistors in the circuit in the targeted area as well as getting only a large amount of the dose (up to ¾ of the dose) to the transistor edge which sits on the trench edge. This will also minimize the counter doping of the source drain with the opposite species as is required by the definition of the halo process.

In the smaller geometries of 0.18 um technologies and lower, the gate height will actually work to advantage and help reduce unwanted counter doping of the source/drain area. In this way the counter doping can be maintained to an absolute minimum. The final advantage is that with the thinner photoresist, we will enhance our ability to provide the implant to smaller geometries.

Accordingly, the process in accordance with the present invention is the improvement in the manufacture-ability as well as enhancing the process capability and device performance and speed.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a flow chart illustrating a conventional process for providing a halo implant.

Figure 2 is a diagram illustrating the semiconductor device after a conventional halo implant.

Figure 3 is a flow chart of a system in accordance with the present invention.

Figure 4 is a diagram illustrating a semiconductor device after a halo implant in accordance with the present invention.

DETAILED DESCRIPTION

The present invention relates to semiconductor devices and more particularly providing a halo implant when manufacturing semiconductor devices. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

Figure 1 is a flow chart illustrating a conventional process for providing a halo implant. Typically in the conventional process, first a thick photoresist is provided, via step 102. Then,

an LDD implant is provided, via step 104. The thick photoresist or LDD mask in a conventional process is typically a photoresist that is 0.55μm in height. After the LDD implant is provided, then we provide what is referred to as the halo implant, via step 106. The halo implant typically is provided at a 45° angle to implant underneath the gate area. For a wafer at a 45° implant, to consistently implant the intended area, a LDD mask is utilized which does not cover the source or drain regions.

Figure 2 is a diagram illustrating the semiconductor device 200 after a conventional halo implant. Accordingly oftentimes the halo implant 202 ends up providing dopant to all of the source region 204 and drain region 206. Since only the area directly underneath the gate 208 is the area of interest for the implant, there is leakage and other problems associated therewith. Accordingly, the entire active area 212 is open primarily because the thickness of the photoresist mask 212 is such that at a 45° angle, the ultraviolet rays cannot accurately be provided underneath the gate area.

As is seen, with a photoresist mask 212 thickness of .5μm, the 45° angle will require that a large portion of the ultraviolet radiation will not reach the area of interest because at that angle, with the thick photoresist, it is not possible. In addition, if a thick photoresist of (0.5μm or greater) is placed over the trench oxidation 207, due to the soft jelly type nature of the photoresist, oftentimes the photoresist will fall over in the trench oxidation area and cover areas that are to be implanted. Even if the photoresist stands erect at the smaller process technologies, the halo implant will not reach the targeted areas.

In a system and method in accordance with the present invention, the implant area is selectively targeted instead of performing a blanket implant. This is accomplished by using a thinner photoresist mask thickness of between 0.1 μm to 0.2 μm instead of 0.55 μm to 0.8 μm

photoresist utilized in the conventional process. To more particularly describe the features of the present invention, refer now to the following discussion in conjunction with the figures.

Figure 3 is a flow chart of a system in accordance with the present invention. Typically as in the conventional process, first a thick photoresist is provided, via step 302. Then, an LDD implant is provided, via step 304. Next, the thick photoresist is removed, via step 306. Thereafter, a thin photoresist is provided, via step 308. Thereafter, a halo implant is provided, via step 310. The halo implant typically is provided at a 45° angle to implant underneath the gate area. For a wafer at a 45° halo implant, to consistently implant the intended area, a LDD mask is utilized which does cover a substantial portion of the source or drain regions.

Figure 4 is a diagram illustrating a semiconductor device 400 after a halo implant in accordance with the present invention. As is shown, the photoresist mask 402 is a smaller height (.1μm to .2μm) than in the conventional process, which allows for more of the source and drain regions 404 and 406 respectively to be masked by the photoresist 402.

Accordingly, in a system and method in accordance with the present invention, a photoresist that is capable of thinner profile, i.e., a DUV photoresist is utilized. This will allow one to lower the photoresist thickness to the proposed 1000A (in the field) or lower if the process allows. With this photoresist thickness, taking into account other height, the source and drain regions can be opened only as needed. At a 45° angle, the implant can be delivered to all transistors in the circuit in the targeted area as well as getting only a large amount of the dose (up to ¾ of the dose) to the transistor edge which sits on the trench edge. This will also minimize the counter doping of the source drain with the opposite species as is required by the definition of the halo process.

In the smaller geometries of 0.18 um technologies and lower, the gate height will

actually work to advantage and help reduce unwanted counter doping of the source and drain region. In this way the counter doping can be maintained to an absolute minimum. The final advantage is that with the thinner photoresist, we will enhance our ability to provide the implant to smaller geometries. Accordingly, the process in accordance with the present invention is the improvement in the manufacture-ability as well as enhancing the process capability and device performance and speed.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one or ordinary skill in the art without departing from the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A method for providing a halo implant to a semiconductor device comprising the steps of:

(a) providing a thin photoresist layer to the semiconductor device; and

(b) providing the halo implant to the appropriate area of the semiconductor device.

2. The method of claim 1 wherein the thin photoresist layer covers a substantial amount of the active area of the semiconductor device.

3. The method of claim 1 wherein the thin photoresist layer is between approximately 0.1 to 0.2μm thick.

4. The method of claim 1 wherein the halo implant is at approximately a 45° angle.

5. The method of claim 1 which includes the step of providing a lightly doped drain implant before the halo implant providing step (b).

6. The method of claim 2 wherein the active area comprises the source region and the drain region of the semiconductor device.

7. The method of claim 1 wherein the photoresist layer comprises a deep

ultraviolet (DUV) layer.

8. A system for providing a halo implant to a semiconductor device comprising:

means for providing a thin photoresist layer to the semiconductor device; and

means for providing the halo implant to the appropriate area of the semiconductor device.

9. The system of claim 8 wherein the thin photoresist layer covers a substantial amount of the active area of the semiconductor device.

10. The system of claim 8 wherein the thin photoresist layer is between approximately 1 to 2μm thick.

11. The system of claim 8 wherein the halo implant is at approximately a 45° angle.

12. The system of claim 8 which includes the step of providing a lightly doped drain implant before the halo implant providing step (b).

13. The system of claim 9 wherein the active area comprises the source region and the drain region of the semiconductor device.

14. The system of claim 8 wherein the photoresist layer comprises a deep ultraviolet (DUV) layer.

ABSTRACT

A method and system for providing a halo implant to a semiconductor device is disclosed. The method and system comprises providing a thin photoresist layer to the semiconductor device. The method and system further includes providing the halo implant to the appropriate area of the semiconductor device. Accordingly, in a system and method in accordance with the present invention, a photoresist that is capable of thinner profile, i.e., DUV photoresist is utilized. This will allow one to lower the photoresist thickness to the proposed 1000A (in the field) or lower if the process allows. With this photoresist thickness, taking into account other height variables, the source and drain regions can be opened only as needed. At a 45° angle, the implant can be delivered to all transistors in the circuit in the targeted area as well as getting only a large amount of the dose (up to ¾ of the dose) to the transistor edge which sits on the trench edge. This will also minimize the counter doping of the source drain with the opposite species as is required by the definition of the halo process.

In the smaller geometries of 0.18 um technologies and lower, the gate height will actually work to advantage and help reduce unwanted counter doping of the source/drain area. In this way the counter doping can be maintained to an absolute minimum. The final advantage is that with the thinner photoresist, we will enhance our ability to provide the implant to smaller geometries.

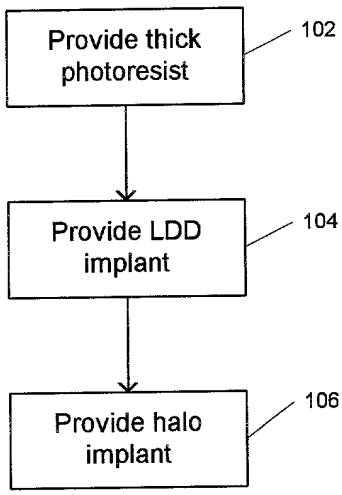
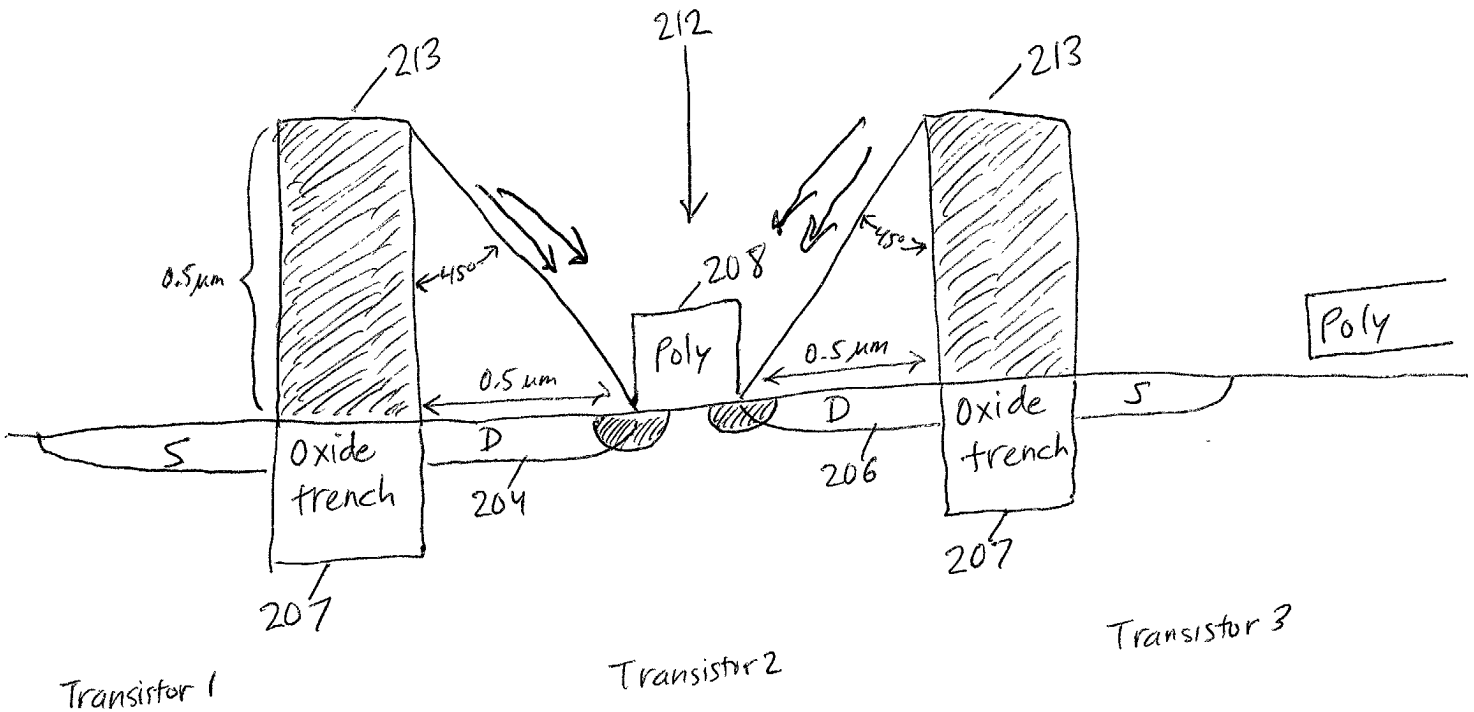

Provide thick photoresist
102
Provide LDD implant
104
Provide halo implant
106

Fig. 1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213
213
0.5 μm
45°
208
Poly
Poly
0.5 μm
0.5 μm
S
Oxide trench
D
204
D
206
Oxide trench
S
207
207
Transistor 1
Transistor 2
Transistor 3

200

Fig. 2

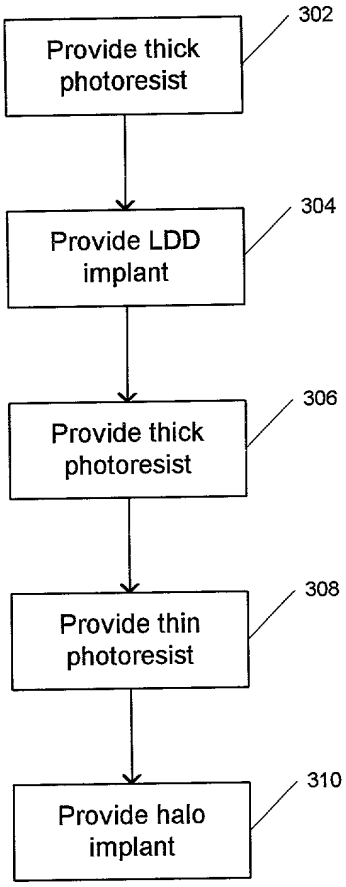
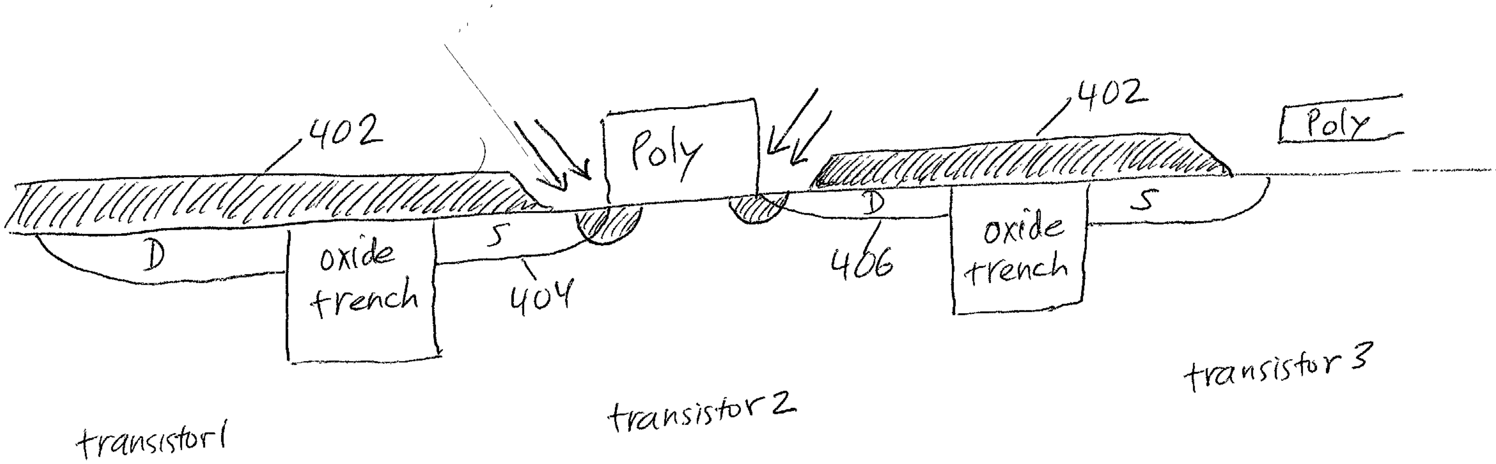

Provide thick photoresist
302
Provide LDD implant
304
Provide thick photoresist
306
Provide thin photoresist
308
Provide halo implant
310

Fig. 3


402
Poly
402
Poly
D
oxide
trench
S
404
D
406
oxide
trench
S
transistor 1
transistor 2
transistor 3

400

Fig. 4

DECLARATION

As the below named inventors, we hereby declare that our residence, post office address and citizenship are as stated below next to our names; that we verily believe we are the original, first and joint inventors of the invention entitled:

METHOD AND SYSTEM FOR PROVIDING HALO IMPLANT TO A SEMICONDUCTOR DEVICE WITH MINIMAL IMPACT TO THE JUNCTION CAPACITANCE

and claiming Benefit under 35 USC 120 of pending United States Provisional Application No. 60/168,155 filed on November 29, 1999, described and claimed in the specification which is attached hereto, that we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above; that we do not know and do not believe the same was ever known or used in the United States of America before our invention thereof, or patented or described in any printed publication in any country before our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by us or legal representatives or assigns more than twelve months prior to this application, that we acknowledge our duty to disclose information of which we are aware which is material to the examination of this application as defined by 37 CFR 1.56(a), and that no application for patent or inventor's certificate on said invention has been filed in any country foreign to the United States of America by us or our legal representatives or assigns.

Address all telephone calls to Mr. Sawyer at telephone number (650) 493-4540 and all correspondence to:

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SAWYER & ASSOCIATES
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Palo Alto, California 94303

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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2-2-00
Date

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Signature of Inventor

DECLARATION (cont.)

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1/25/00
Date

Signature of Inventor

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Citizenship: **United States of America**

31 Jan 2000
Date

Signature of Inventor

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: **Ahmad Ghaemmaghami; Zoran Krivokapic; Brian Swanson**

Title: **METHOD AND SYSTEM FOR PROVIDING HALO IMPLANT TO A SEMICONDUCTOR DEVICE WITH MINIMAL IMPACT TO THE JUNCTION CAPACITANCE**

POWER OF ATTORNEY BY ASSIGNEE AND EXCLUSION OF INVENTOR UNDER 37 C.F.R. SEC. 1.32

Honorable Commissioner of Patents and Trademarks
Box Patent Applications
Washington, D.C. 20231
Sir:

ADVANCED MICRO DEVICES, Inc., a Delaware Corporation, having become the owner of all rights in and to the above-identified application by virtue of an Assignment executed by the inventor concurrently with the execution of the application, said Assignment being submitted herewith for recording, hereby appoints:

Vincenzo D. Pitruzzella, Reg. No. 28,656
Richard J. Roddy, Reg. No. 27,688
William D. Zahrt, II, Reg. No. 26,070
Paul S. Drake, Reg. No. 33,491
Louis A. Riley, Reg. No. 39,817
Wendell J. Jones, Reg. No. P45,961
Elizabeth A. Apperley, Reg. No. 36,428
Joseph A. Sawyer, Jr., Reg. No. 30,801
Janyce R. Mitchell, Reg. No. 40,095
Stephen G. Sullivan, Reg. No. 38,329
Michele Liu, Reg. No. 44,875

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their attorneys, to prosecute said application and to transact in connection therewith all business in the Patent and Trademark Office and before competent International Authorities; said appointment to be to the exclusion of the inventor and his attorneys in accordance with the provisions of 37 C.F.R. 1.32.

Date: 2 February, 2000

William D. Zahrt II

Name: William D. Zahrt II
Title: Assistant General Counsel